AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Canceled)

2. (Currently Amended) A method of calculating, by the use of a computer, a numerical value V_A and a degraded V_A representative of a circuit property of a logic level circuit, V_A is calculated from a numerical value V_B, which shows a block property of a logic block included in the logic level circuit, the method comprising:

(a) calculating the value V_B from a plurality of numerical values V_C, each value V_C of the plurality of numerical values V_C representing a transistor property of a transistor ~~included~~ in the logic block; and;

(b) calculating the value V_A from the value V_B, and outputting the value V_A as a value representative of the~~a~~ circuit property of said logic level circuit,

wherein, in the step (a), the plurality of values V_C comprises ~~only~~ a first V_C value that shows a property of a transistor connected directly to an input pin of the logic block and a second V_C value that shows a property of a transistor connected directly to an output pin of the logic block, and

wherein only the first V_C and the second V_C are used in calculating a degradation delay and wherein a degraded V_A is calculated from the V_A and the calculated degradation delay.

3. (Currently Amended) A method of calculating, by the use of a computer, a delay time of a signal passing through a logic level circuit which consists of a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time, which is delay time of a signal passing between two logic blocks connected to each other, comprising:

(a) calculating the pin-to-pin delay time~~,~~ based on a value of a transistor property of a transistor included in the logic block, and the block-to-block delay time without calculating in aging ~~caused by hot carrier effect~~;

(b) calculating variations of signal delay times caused by aging based on V_C values, wherein for calculating the signal delay times caused by aging ~~comprising exclusively a transistor property of~~ an age delay of a transistor connected directly to the input pin and ~~a transistor property of~~ a transistor connected directly to the output pin is used; and~~,~~

(c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b), and outputting said modified values for use as values representative of circuit properties of said logic level circuit.

4. (Currently Amended) A method of calculating, by the use of a computer, pin-to-pin delay time T_{iopath_aged}, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time $T_{connect\_aged}$, which is delay time of a signal passing between said two logic blocks connected to each other, comprising:

(a) calculating an amount of stress S_{in} cast by the input pin and an amount of stress S_{out} cast by the output pin according to the following expression:

$$S = \alpha\left(\frac{C}{W}\right)^{\beta}$$

where a load capacitance is represented by C [pF], constants depending on change of inputted waveform are represented by α and β, and width of channel of the transistor connected to the pin is represented by W [μm];

(b) calculating an aged delay time of the input pin δin [%] and an aged delay time δout [%] according to the following expression:

$$\delta = \gamma\left(\frac{\tau Sf}{\varepsilon_1 e^{\kappa T}}\right)^{\frac{1}{\varepsilon_2}}$$

where a constant depending on physical structure of the pin is represented by γ, the term of guarantee of the LSI is represented by τ [hour], constants depending on process are

represented by ε1, ε2 and κ, working frequency is represented by f [Hz], and absolute temperature is represented by T [K];

(c) calculating and outputting for use as values representative of circuit properties of said logic level circuit the pin-to-pin delay time T_{iopath_aged} and the block-to-block delay time $T_{connect\_aged}$ according to the following expressions:

$$T_{iopath\_aged} = T_{iopath\_fresh}\left(1 + \lambda_{in}\delta_{in} + \lambda_{out}\delta_{out}\right)$$
$$T_{connect\_aged} = T_{connect\_fresh}\left(1 + \lambda_{out}\delta_{out}\right)$$

where pin-to-pin delay time and block-to-block delay time calculated ignoring aging caused by hot carrier effect are represented by T_{iopath_fresh} [ps] and $T_{connected\_fresh}$ [ps], and ratios of delay times ~~degradations~~ occurred at the input stage and the output stage to whole delay time occurred from the input pin to the output pin are represented by λin and λout.

5. (Previously Presented) A method of calculating, by the use of a computer, a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, comprising:

(a) calculating delay times of all said logic blocks according to the method as in claim 3; and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a).

6. (Currently Amended) A method of calculating, by the use of a computer, a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, comprising:

(a) calculating delay times of all said logic blocks according to the method as in claim 4; and~~,~~

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a).

7. (Canceled)

8. (Currently Amended) A computer-readable medium incorporating a program of instructions for calculating a numerical value V_A, which shows a property of a logic level circuit, from a numerical value V_B, which shows a property of a logic block constituting the logic level circuit, the program making a computer execute the following processes:

(a) calculating the V_B value from a plurality of numerical values V_C, each V_C value showing a property of a transistor constituting part of the logic block;

(b) calculating an aged V_B from the V_B calculated in step (a) and an aged delay time of only a first V_C and a second V_C, and,

(b) calculating the V_A value from the degraded V_B value, and outputting the V_A value for use as a value representative of ~~a~~ the circuit property of said logic level circuit,

wherein ~~in process (a) the plurality of V_C values comprises exclusively a~~ the first V_C is a degradation delay time value of a transistor connected directly to an input pin of the logic block and ~~another~~ the second V_C is a degradation delay time value of a transistor connected directly to an output pin of the logic block.

9. (Previously Presented) A computer-readable medium incorporating a program of instructions for calculating a delay time of a signal passing through a logic level circuit which includes a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time, which is delay time of a signal passing between two logic blocks connected to each other, the program configured to make a computer execute the following processes:

(a) calculating the pin-to-pin delay time and the block-to-block delay time without calculating in aging caused by hot carrier effect;

(b) calculating variations of signal delay times caused by aging, based on transistor property values only for transistors inside the logic block connected directly to one of the input pin and the output pin of the logic blocks; and,

(c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b), and outputting said modified values for use as values representative of circuit properties of said logic level circuit.

10. (Currently Amended) A computer-readable medium incorporating a program of instructions for calculating, by using a computer, pin-to-pin delay time T_{iopath_aged}, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time $T_{connect\_aged}$, which is delay time of a signal passing between said two logic blocks connected to each other ~~by a computer~~, the program making a computer execute the following processes:

(a) calculating an amount of stress S_{in} cast by the input pin and an amount of stress S_{out} cast by the output pin according to the following expression:

$$S = \alpha\left(\frac{C}{W}\right)^{\beta}$$

where a load capacitance is represented by C [pF], constants depending on change of inputted waveform are represented by α and β, and width of channel of the transistor connected to the pin is represented by W [μm];

(b) calculating an aged delay time of the input pin δ_{in} [%] and an aged delay time δ_{out} [%] according to the following expression:

$$\delta = \gamma \left(\frac{\tau S f}{\varepsilon_1 e^{\kappa T}} \right)^{\frac{1}{\varepsilon_2}}$$

where that a constant depending on physical structure of the pin is represented by γ, the term of a guarantee of the LSI is represented by τ [hour], constants depending on process are represented by $\varepsilon 1$, $\varepsilon 2$ and κ, working frequency is represented by f [Hz], and absolute temperature is represented by T [K];

(c) calculating and outputting for use as values representative of circuit properties of said logic level circuit the pin-to-pin delay time T_{iopath_aged} and the block-to-block delay time $T_{connect\_aged}$ according to the following expressions:

$$T_{iopath\_aged} = T_{iopath\_fresh}\left(1 + \lambda_{in}\delta_{in} + \lambda_{out}\delta_{out}\right)$$
$$T_{connect\_aged} = T_{connect\_fresh}\left(1 + \lambda_{out}\delta_{out}\right)$$

where pin-to-pin delay time and block-to-block delay time calculated ignoring aging caused by hot carrier effect are represented by T_{iopath_fresh} [ps] and $T_{connected\_fresh}$ [ps], and ratios of delay times ~~degradations~~ occurred at the input stage and the output stage to whole delay time occurred from the input pin to the output pin are represented by λ_{in} and λ_{out}, respectively.

11. (Previously Presented) A computer-readable medium incorporating a program of instructions for calculating a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, the program making a computer execute the following processes:

(a) calculating delay times of all said logic blocks according to the program as in claim 9; and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a).

12. (Previously Presented) A computer-readable medium incorporating a program of instructions for calculating a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, the program making a computer execute the following processes:

(a) calculating delay times of all said logic blocks according to the program as in claim 10; and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a).

13. (Currently Amended) A signal delay calculation system which calculates the delay time of a signal passing through a logic level circuit consisting of a plurality of logic blocks, the system comprising:

first calculation means for calculating value V_B, a property of a logic block constituting the logic level circuit, based on a plurality of numerical values V_C, each V_C value representing a property of a transistor included in the logic block;

second calculation means for calculating an aged value V_B from the value V_B and a delay degradation time of a first value V_C and a second value V_C;

third calculation means for calculating a value V_A representing a signal delay property of a logic level circuit, from ~~value~~ an aged value V_B; and

output means for outputting value V_A,

wherein ~~in the first calculation means, the plurality of V_C values includes exclusively a~~ the first V_C is a value of a transistor connected directly to an input pin of the logic block and ~~a~~ the second V_C is a value of a transistor connected directly to an output pin of the logic block.

14. (Previously Presented) The system of claim 13, wherein V_A is an aging delay property of a logic level circuit.

15. (New) A method of calculating by a computer an aged delay time of a circuit having a plurality of logic blocks, each block having a plurality of transistors, the method comprising:

calculating a delay time of a fresh circuit;

calculating a degradation delay time of a transistor directly connected to an input pin and of a transistor directly connected to an output pin of said each logic block; and

calculating the aged delay time of the circuit using the calculated degradation delay time and the delay time of the fresh circuit.

16. (New) The method according to claim 15, wherein the degradation delay time is calculated using a delay time degradation rate and wherein the degradation delay time is caused by a hot electron effect.